Ahmedabad University

School of Arts and Sciences

CSC201 Computer Organization

BS(Hons) in CS
Mid Term Examination 2022-23 (Monsoon Semester)

Total Marks = 100 **Time – 2 hours**

Enrolment Number:.....
Date: 20-09-2022
No. of printed pages: 2

1. marks: 5
Convert the following two's complement binary numbers to decimal. Show your work
(b) 100011_2 (c) 01001110_2

2. marks: 5
Convert the following decimal numbers to 8-bit two's complement numbers or indicate that the decimal number would overflow the range.
(b) -59_{10} (d) -150_{10}

3. marks: 10
Simplify the following Boolean expressions to a minimum number of literals:
(a) $(a + b + c')(a'b' + c)$
(b) $a'bc + abc' + abc + a'bc'$

4. marks: 10
Determine whether the following Boolean equation is true or false.
$a'd' + b'c' + c'd' = (a' + c')(b' + d')(c' + d')$
Show your work.

5. marks: 10
A *majority gate* produces a TRUE output if and only if more than half of its inputs are TRUE. Complete a truth table for the three-input majority gate and find a minimized boolean expression using essential prime implicants.

6. marks: 10

Write the minimized equation in sum-of-products form for each of the following truth table and sketch a *reasonably simple* combinational circuit using NAND gates only. Here X represents the set of minterms with don't-care conditions. Reasonably simple means that you are not wasteful of gates, but you don't waste vast amounts of time checking every possible implementation of the circuit either.
$F(A, B, C, D) = \Sigma(1, 8, 11, 13, 15)$
$X(A, B, C, D) = \{2, 3, 5, 6, 7, 14\}$

7. marks: 10

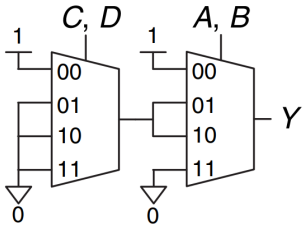
A circuit has four inputs and two outputs. The inputs A3:0 represent a number from 0 to 15. Output P should be TRUE if the number is prime (0 and 1 are not prime, but 2, 3, 5, and so on, are prime). Output D should be TRUE if the number is divisible by 3. Give simplified Boolean equations for each output and sketch a reasonably simple circuit.

8. marks: 10

Implement the equation $Y = BC + A'B'C' + BC'$ using an 8x1 Mux

9. marks: 10

Write a minimized Boolean equation for the function performed by the circuit in the figure below.



10. marks: 10

The *Toggle* (T) flip-flop has one input, CLK, and one output, Q. On each rising edge of CLK, Q toggles to the complement of its previous value. Draw a schematic for a T flip-flop using a D flip-flop and an inverter.

11. marks: 10

Given the input wave-forms shown in the figure below, sketch the output, Q, of an SR latch.

